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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **05 / 11 / 2024** | **Batch No:** | **C3** |
| **Faculty Name:** | **Bharathi Narayan** | **Roll No:** | **16010123217** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 8**

**Title: 1-bit adder on VHDL**

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| **Aim and Objective of the Experiment:** |
| To implement 1-bit adder on VHDL |

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| **COs to be achieved:** |
| **CO4**: Implement digital networks using VHDL |

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| **Tools used:** |
| Quartus, ModelSim |

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| **Theory:** |
| A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input.  Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems. |

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| **Implementation Details** |
| Code:    Output: |
| **Post Lab Subjective/Objective type Questions:** |
| 1. How can 1-bit adder be used to implement a 4-bit adder?   Ans. To implement a 4-bit adder using 1-bit adders, you would chain four 1-bit full-adders together to create a 4-bit ripple carry adder. Each 1-bit full-adder will handle the addition of a single bit from each of the two 4-bit numbers. The carry-out from each 1-bit adder is connected to the carry-in of the next higher-order bit.  Working:   1. Each bit position (from least significant to most significant) is handled by a separate 1-bit full-adder. 2. For the first bit (least significant bit), the carry-in (Cin) is usually set to 0. 3. The output Sum from each 1-bit full-adder is one bit of the final result. 4. The carry-out from each full-adder becomes the carry-in for the next higher bit position. 5. The carry-out from the final (most significant) bit position can indicate an overflow. 6. What is VHDL used for?   Ans. VHDL (VHSIC Hardware Description Language) is used to describe the behavior and structure of electronic systems, particularly digital logic circuits, in a way that is machine-readable. It’s primarily used in:   1. **Digital Circuit Design**: VHDL helps design digital components, such as adders, multiplexers, registers, counters, and more complex circuits like processors. Engineers use it to specify how these components should function and interact. 2. **Simulation and Verification**: VHDL allows for the simulation of digital circuits before physically implementing them, ensuring the design works as intended. Designers can verify logic correctness, timing, and other parameters in software before hardware synthesis. 3. **Synthesis of Hardware**: VHDL code can be synthesized into a netlist that specifies connections and logic gates, which can be further used to create real hardware in FPGA (Field Programmable Gate Array) or ASIC (Application-Specific Integrated Circuit) technologies. 4. **Reusable Hardware Modules**: VHDL promotes modular design, allowing the development of reusable and parameterized hardware components that can be used across different projects. |

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| **Conclusion:** |
| From this experiment, we learnt how to code a 1-bit adder using full adder in VHDL |

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| **Signature of faculty in-charge with Date:** |